IN THE CLAIMS:

Please amend the claims as follows.

1. (Currently Amended) A bridge comprising:

a plurality of interface registers that are configured to facilitate communication of data with a plurality of function units, and

a plurality of register transfer units, operably coupled to the plurality of interface registers, that facilitate transfers of data among at least two interface registers of the plurality of interface registers.

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2. (Previously Amended) The bridge of claim 1, further comprising:

an instruction memory that is configured to contain register transfer instructions, and

wherein the operable coupling of the plurality of register transfer units and the plurality of function units is effected via the register transfer instructions.

3. (Previously Amended) The bridge of claim 1, further comprising:

at least one datapath unit, operably coupled to the plurality of register transfer units, that facilitates a transformation of at least one data item of the data that is transferred among the interface registers.

4. (Previously Amended) The bridge of claim 3, further comprising:

an instruction memory that is configured to contain register transfer instructions, and

wherein the operable coupling of the plurality of register transfer units and the plurality of function units and the at least one datapath unit is effected via the register transfer instructions.

5. (Previously Amended) The bridge of claim 1, wherein:

at least one of the function units is a programmable digital signal processor.

6. (Previously Amended) A signal processing system comprising:

a receiver that is configured to provide a digital input stream,

a channel decoder, operably coupled to the receiver, that is configured to decode the digital input stream into a decoded signal stream, and

a user application, operably coupled to the channel decoder, that is configured to render an output corresponding to a channel of the digital input stream based on the decoded signal stream,

wherein the channel decoder comprises a bridge comprising:

a plurality of interface registers, each associated with a processing unit of a plurality of processing units, and

a plurality of register transfer units, operably coupled to the plurality of interface registers, that facilitate:

transfers of data among interface registers of the plurality of interface registers,

transfers of data of the digital input stream among interface registers of the plurality of interface registers, and

transfers of data from the interface registers to provide the decoded signal stream.

7. (Previously Amended) The signal processing system of claim 6, wherein the channel decoder further comprises:

an instruction memory that is configured to contain register transfer instructions, and

wherein the operable coupling of the plurality of register transfer units and the plurality of processing units is effected via the register transfer instructions.

8. (Previously Amended) The signal processing system of claim 6, further comprising:

at least one datapath unit, operably coupled to the plurality of register transfer units, that facilitates a transformation of at least one data item of the data that is transferred among the interface registers.

9. (Previously Amended) The signal processing system of claim 8, wherein the channel decoder further comprises:

an instruction memory that is configured to contain register transfer instructions, and

wherein the operable coupling of the plurality of register transfer units and the plurality of processing units and the at least one datapath unit is effected via the register transfer instructions.

10. (Previously Amended) The signal processing system of claim 6, wherein:

at least one of the processing units is a programmable digital signal processor.

11. (Previously Added) A method, comprising:

receiving data at a plurality of interface registers, the interface registers operable to communicate with a plurality of function units;

allowing at least one of the function units to process the data in at least one of the interface registers;

communicating the data among at least two of the interface registers using a plurality of register transfer units; and

allowing at least one of the function units to further process the data in at least one of the interface registers.

12. (Previously Added) The method of Claim 11, wherein communicating the data among at least two of the interface registers comprises using register transfer instructions in an instruction memory to communicate the data among at least two of the interface registers.

13. (Previously Added) The method of Claim 11, further comprising transforming at least one data item of the data that is transferred among the interface registers.

14. (Previously Added) The method of Claim 11, wherein at least one of the function units is a programmable digital signal processor.

15. (Previously Added) The method of Claim 11, wherein receiving data comprises receiving a digital input stream from a receiver.

16. (Previously Added) The method of Claim 15, further comprising generating a decoded signal stream using the digital input stream.

17. (Previously Added) The method of Claim 16, further comprising communicating the decoded signal stream to a user application operable to render an output corresponding to a channel of the digital input stream based on the decoded signal stream.